***EE/CprE/SE 492 BIWEEKLY REPORT 04***

**Date:** October 12, 2022 – October 25, 2022

**Group number:**  Dec2022-20

**Project title:** i281 CPU Hardware Implementation

**Client &/Advisor:** Dr. Alexander Stoytchev

**Team Members/Role:**

Alex Kiefer (Hardware Team)

David Vachlon (Software Team)

Joseph De Jong (Hardware Team)

Saffron Edwards (Software Team)

 Patrick O’Brien (Hardware Team)

**Summary**

Our team completed the breadboard implementation and started debugging. Debugging is a slow activity that requires the creation of test benches, unwiring/rewiring, and patience. Later in the report, we will discuss our findings and solutions.

The PCB clock arrived and was soldered together. This clock will help reduce noise while debugging, as we have one less variable to worry about. Additionally, the other PCBs were finalized and are ready for implementation.

**Past Week Accomplishments**

* **Alex Kiefer:** Finished the Program Counter PCB, as well as finalized changes to the Register File PCB.
* **David Vachlon:** Worked on finishing wiring the EEPROM modules. Helped Joe wire the connections between modules. Continued to handle ordering requested components.
* **Joseph De Jong:** Joe helped wire all the breadboards together to create a datapath. Upon completion, goals and test benches were set up to prepare for adding power to the system. A large set of these test benches failed and are being reworked to meet specifications.
* **Saffron Edwards:** Assisted with breadboard datapath wiring and took on project manager role to better suit the team.
* **Patrick O’Brien:** Worked on the ALU and switchboard PCBs. Helped Joe to arrange and wire the breadboards.

**Pending Issues**

* **David Vachlon:** Decisions still need to be made on if more software will need to be written to support this CPU in the future.
* **Alex Kiefer:** Create the Bus Mux PCB and all of their variants. Need to fix PCB design for register file
* **Joseph De Jong:** The CPU implementation did not pass all test benches required for boot. These issues will need to be resolved before moving forward.
* **Patrick O’Brien:** Need to create BOM for the PCB design for pricing. Need to finish the ALU design.
* **Saffron Edwards:** Talking with David and Dr. Stoytchev about any software components still needed along with future project management requirements.

**Individual Contributions**

| **NAME**  | **Individual Contributions**  | **Hours this** **week** | **HOURS** **cumulative** |
| --- | --- | --- | --- |
| Alex Kiefer | Program Counter PCB |  4 | 42 |
| David Vachlon | EEPROM wiring and module connection wiring | 5 | 44 |
| Joseph De Jong | Building breadboard datapath/ CPU | 5 | 44 |
| Saffron Edwards | Breadboard help and software discussions | 3 | 26 |
| Patrick O’Brien |  ALU and switchboard PCB | 5 | 44 |

**Plans for the Coming Week**

* **Hardware:** Meet all test bench requirements so that a data test can be completed. These tests will require troubleshooting and modifications.

While the datapath is being completed, PCBs are being finalized for purchasing and printing. Each PCB will need to be soldered together upon arrival.

* **Software:** Discussing with the client potential software support ideas/if the client needs any more software written to support the CPU in the future.

**Summary of Weekly Advisor Meeting**

The last two weeks of advisor meetings covered various issues. These include:

* Picking data connection types between PCBs: A 10-pin ribbon cable design will be used to link data between modules. Many modules may require more than one ribbon cable.
* Picking a power, ground, clock, reset wire style. A Molex-style wire will be used to carry these signals to protect signal integrity.
* Bux Mux PCB design - where each mux will be placed and what modules will require an individual bus mux.

Each member discussed their concerns on the topics listed above. Eventually, a consensus was found, and design choices were implemented.